A Study of Optimal Matching Circuit Topologies for Broadband Monolithic Power Amplifiers

by

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Abstract

A large signal amplifier design technique for broadband monolithic amplifiers has been expanded to include studies of the optimal output circuit topology from the standpoint of large and small signal gain variations and stability.

Introduction

The main objective behind the development of GaAs monolithic amplifiers is to provide an inexpensive microwave amplifier on a chip. To the circuit designer, size is of primary importance in reducing amplifier cost. The smaller an amplifier can be made to perform a given function the more amplifier chips can be obtained from a given size wafer. For wideband amplifiers operating below 10 GHz, this desire to minimize overall chip size effectively precludes the commonly used balanced amplifier approach to wideband performance since such an approach requires relatively large quadrature couplers on the input and output of each stage in addition to matched amplifier pairs.

Design Approach

An alternate single ended approach has been described recently which is based on load-pull characterization of the FET devices and has been used to design several 5-10 GHz two stage monolithic power amplifiers. This approach basically consists of placing the full 6 dB/octave gain equalization burden for each FET onto the circuitry immediately following that particular FET. This allows the input of the amplifier to be flatly matched across the band thereby retaining, a least to some degree, the good input match advantage of a balanced amplifier. This alternate approach may be summarized as follows.

1. For a given fixed input power level, load pull contours are plotted corresponding to constant power output at each frequency.
2. The output circuit (or interstage circuit in the case of the first stage) is designed to present an impedance locus which crosses these constant power contours in a manner to provide constant power at each frequency.

Thus, the output circuit provides the optimum load impedance at the highest frequency of interest while selectively "de-optimizing" the load impedance at lower frequencies to provide constant power (and gain).

For the 2400-μ Westinghouse FET's used in the output stage of the aforementioned 5-10 GHz amplifiers a typical set of load-pull data is shown in fig. 1(a), while a typical set of composite load-pull curves, representing constant power output, gain and to a first approximation constant efficiency at each frequency is shown in fig. 1(b). Also shown in fig. 1(b) is the impedance locus that the output circuit presents to the FET illustrating the manner in which it crosses the load pull curves to produce flat output power.

Matching Circuits

Examination of fig. 1(b) immediately raises important questions; e.g., for the many possible output circuit configurations and resulting impedance loci, is there an optimum configuration, and secondarily what are the tradeoffs between large and small signal gain and stability for the various configurations? In order to gain insight into this problem,

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a study of 12 three, four and five element output matching circuits for a 2400μ single stage amplifier has been made to ascertain differences in large and small signal gain performance and stability. The number of circuits studied was reduced from 55 to 12 by restricting the analysis to biasable circuits; i.e., those having a shunt inductance to ground at the drain end of the circuit (thru which drain bias can be injected) and a series capacitor to block the bias from the 50Ω load.

The results of this study may be summarized by examining the performance of four typical circuits and their associated impedance loci as shown in fig. 2. Notice that all the loci result in nearly the same large signal performance as shown by the large signal gain vs. frequency curves of fig. 3. However, under small signal conditions as shown in fig. 4 there are significant differences in gain ($\simeq$ 4 dB) close to the lower band edge, with circuit "D" giving the smallest gain increase under small signal conditions.

All of the circuits are unconditionally stable in the band of interest, however there are important differences below 5 GHz as shown in fig. 5. This figure compares the impedance loci for the circuits below 5 GHz with the stability circles for the various frequencies as indicated. Note the circuit "D" is unstable below 2 GHz, whereas circuits, "A", "B" and "C" are stable. Hence, while circuit "D" yields the flattest small signal gain, its instability below 2 GHz makes it unusable (at least in its present form). Any of the three other circuits are acceptable from the stability standpoint, however circuits "B" and "C" have the most reasonable capacitor values (for fabrication in an interdigital format). A variation of circuit "B" was used in the 1200μm/2400μm two stage amplifier discussed in the next paragraph.

Two Stage Power Amplifier

This design approach has been used to fabricate two "lumped element" two stage 5-10 GHz amplifiers. The first , shown in fig. 6, incorporates a 900μm FET in the first stage and a 2400μm FET in the second. Matching circuits utilize interdigital capacitors and inductors formed by short lengths of transmission line. Vias have also been incorporated for improved source grounding (lower inductance) and to provide circuit flexibility. This amplifier produced 28$\pm$0.7dBm output power with 6$\pm$0.7dB associated gain from 5.5 to 11.0 GHz.

The second amplifier incorporates a 1200μ FET in the first stage followed again by a 2400μ FET in the second. This amplifier, currently in processing, is calculated to have an output power of 1 watt over the band. Results on this amplifier will be presented at the symposium.

Conclusions

An experimentally verified broadband power amplifier design procedure, has been expanded so that a number of possible large signal designs can be conveniently compared on the basis of (1) the number of circuit elements required and their magnitude, (2) gain variations from rated RF drive power down to small signal drive, and (3) stability conditions. Although it was only illustrated for the design of the output circuit, the expanded technique is also applicable to the design of interstage circuits.

Acknowledgment

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Reference

1. J. E. Degenford, R. G. Freitag, D. C. Boire and M. Cohn, "Design Considerations for Wideband Monolithic Power Amplifiers", 1980 GaAs IC Symposium Digest, Las Vegas, Nevada; Nov. 4-6, 1980.

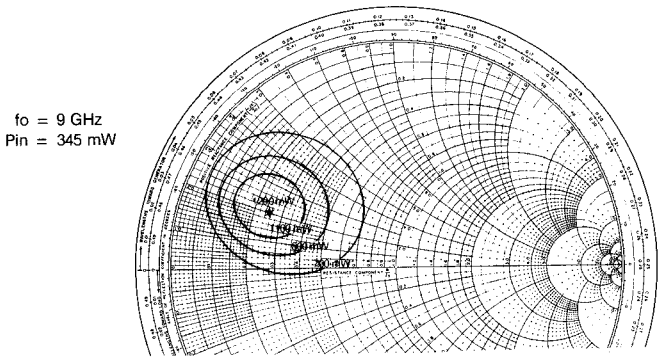

Fig. 1a. Typical load-pull data for 2400 μm FET.

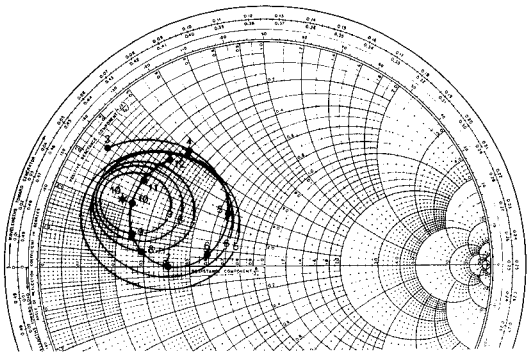

Fig. 1b. Output stage impedance locus for two stage monolithic amplifier.

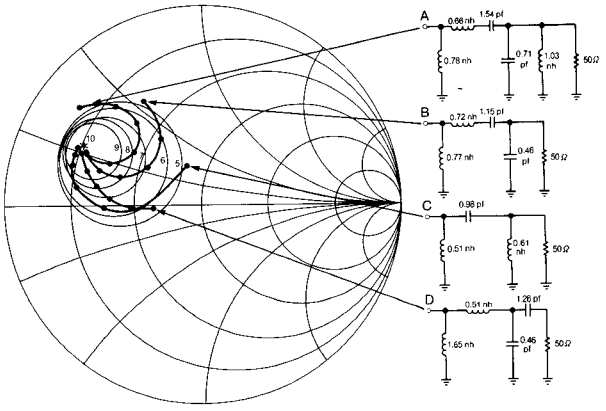

Fig. 2. Four output circuits and their corresponding impedance loci from 5 to 10 GHz superimposed on composite 2400 μm FET load pull contours.

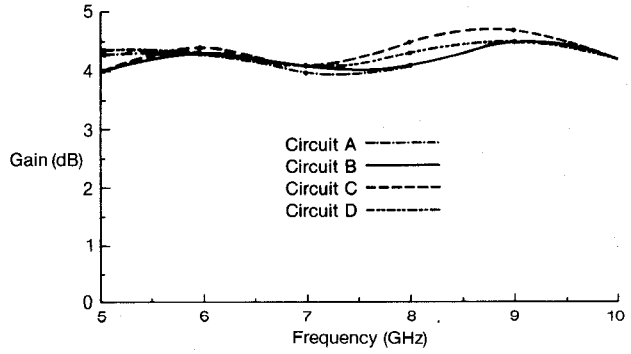

Fig. 3. Large signal 2400 μm amplifier gain.

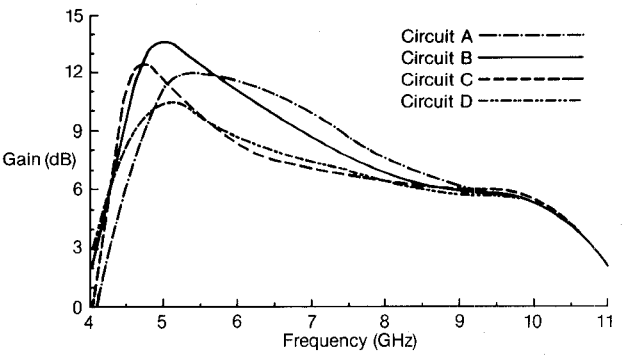

Fig. 4. Small signal 2400 μm amplifier gain.

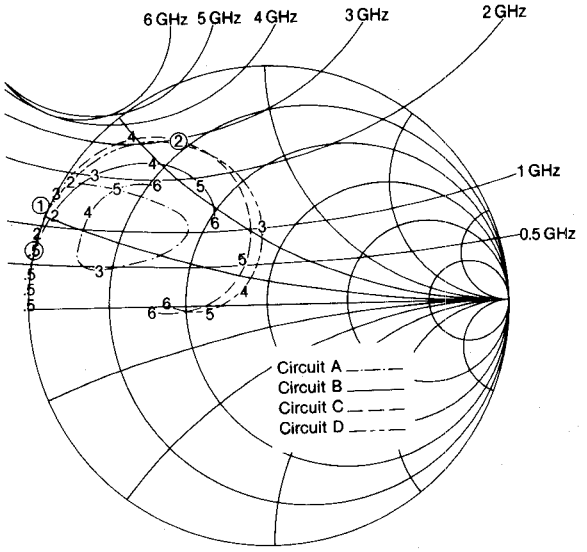

Fig. 5. Output plane stability circles for the 2400 μm FET and the corresponding impedance loci of the four output circuits under consideration. Stable regions are outside the circles. Unstable points are circled.

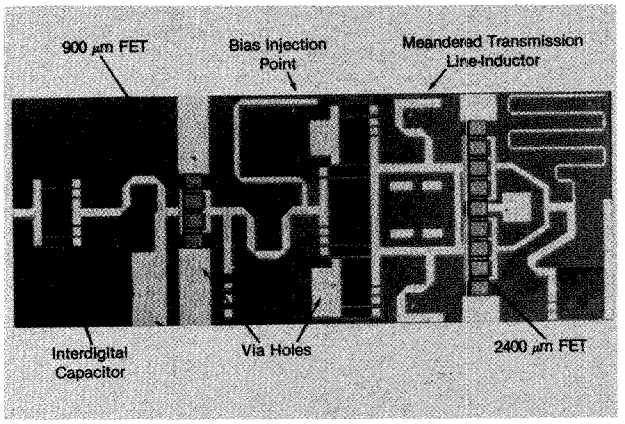

Fig. 6. Two stage monolithic GaAs octave bandwidth (5.5-11.0 GHz) power amplifier. Chip size is 80 mils by 190 mils.